

What is claimed is:

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*50* 1. A data input/output (I/O) system connected to an address bus and a data bus, comprising:

a first register that stores data from the data bus in response to an access signal supplied from the address bus; and

a memory that receives the data stored in the first register and inputs and outputs data from and to the data bus using the data as an address signal.

10 2. The data I/O system of claim 1, further comprising an address generation circuit that generates an address signal accessible by the memory and supplies the address signal to one of the memory and the first register.

15 3. The data I/O system of claim 2, further comprising a second register connected between the memory and the data bus for storing data from one of the data bus and the memory in response to the access signal.

20 4. The data I/O system of claim 3, further comprising a digital-to-analog (D/A) converter that receives data from the second register and converts the data to an analog signal.

25 5. The data I/O system of claim 4, wherein the address generation circuit generates a circulating address signal, and the D/A converter generates the analog signal having a periodic waveform by repetitively receiving data from the second register.

30 6. The data I/O system of claim 2, wherein the address generation circuit includes:

a counter that counts clock signal pulses and generates the

address signal, which corresponds to the count value;

a control register that stores an end address of the data stored in the memory; and

5 a comparator connected to the counter and the control register to compare the end address and the address signal and supply a signal for resetting the count value of the counter when the end address and the address signal match.

10 7. The data I/O system of claim 6, wherein the counter is an up-and-down counter that performs one of an incremental count operation and a decremental count operation in response to a switching signal, and the up-and-down counter resets the count value in response to a clear signal in the incremental count operation and sets the end address to the initial value in the  
15 decremental count operation when the count value has underflowed.

8. The data I/O system of claim 1, further comprising:  
a decoder connected to the address bus to generate a control  
signal in response to the access signal; and  
20 a switch circuit connected between the memory and the data bus and being conductive in response to the control signal.

9. A data I/O system, comprising:  
an analog-to-digital (A/D) converter that converts an  
25 analog signal to a digital signal;  
a memory connected to the A/D converter that stores the digital signal;  
a register connected to the memory that stores an address signal; and  
30 an address generation circuit connected to the register that generates the address signal and supplies the address signal to the register.

10. A data I/O system, comprising:  
a first function block including,  
a first register that stores a first address signal,  
5 a first memory that receives the first address signal  
stored in the first register and inputs and outputs data in  
accordance with the first address signal,  
a first address generation circuit that generates the  
first address signal successively and supplies the first address  
10 signal to the first register, and  
a digital-to-analog (D/A) converter that receives data  
from the first memory and converts the data to an analog signal;  
a second function block connected to the first function  
block, including,  
15 an analog-to-digital (A/D) converter that converts the  
analog signal to a digital signal,  
a second memory that stores the digital signal,  
a second register connected to the second memory that  
stores a second address signal, and  
20 a second address generation circuit connected to the  
second register that generates the second address signal  
successively and supplies the second address signal to the second  
register; and  
a processor that receives the digital signal from the second  
25 memory, corrects the data stored in the first memory, and supplies  
the corrected data to the first memory.

11. A method for inputting and outputting data, comprising  
the steps of:  
30 storing an address signal from an address bus in a register;  
writing data to a storage device in accordance with the  
address signal stored in the register;

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